Amendments to the Specification:

Please amend paragraph [0039] as follows:

Turning to FIGURE 1, the source and drain region 14 is formed by performing an ion implantation to dope ions into the substrate 2 using the gate structure 6 and sidewall spacers 12 as a mask. After selectively etching isolation layer 10, portions of the gate 6 and substrate 2 are exposed. Silicide 16 is introduced on the exposed surface of the top portion of gate and the silicon substrate 2 on the source and drain regions 14 to reduce their resistance. Preferably, the silicide 16 can be TiSi2, CoSi2 or NiSi. The gate structure 6 acts as the control gate, and the nitride spacers are used to trap carriers. The spacers 12 may be used to store charges, thereby defining the digital states including (0, 0), (0, 1), (1, 0), (1, 1). A sectional view of a multi-bit nonvolatile memory cell in accordance with the present invention is shown in FIG. 1-24. The memory cell includes a substrate 2 having at least two buried PN junctions, one is the left junction and the other is the right junction. Channels are located between the two junctions during operation. Above the main channel is an oxide 4, on top of the oxide layer 4 is a control gate 6. Spacer 12 is used for charge trapping and is preferably comprised of silicon nitride. The hot electrons or holes are trapped as they are injected into the Spacer 12 from the injection portion near source/drain to channel junction throughout the isolation layer 10 over the substrate 2.